

MOUNTING FOR A PACKAGE CONTAINING A CHIP

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10 BACKGROUND

1. Field of the Invention

The present invention relates to a mounting for a package containing a semiconductor chip.

2. Description of the Related Art

15 A typical package for a semiconductor chip includes an internal leadframe, which functions as a substrate for the package. The leadframe includes a central metal die pad and a plurality of leads. A body of a hardened, insulative encapsulant material covers the die, die pad, and an inner portion of each of the leads. The encapsulant material is provided both above and below the die pad and leads.

20 The semiconductor chip is mounted on the die pad and is electrically connected to the leads. In particular, the chip includes a plurality of bond pads, each of which is electrically connected by a conductor (e.g., a bond wire) to an encapsulated inner portion of one of the leads. An outer portion of each lead extends outward from the body of encapsulant material, and serves as an input/output terminal for the package. The outer
25 portion of the leads may be bent into various configurations, such as a J lead configuration or a gull wing configuration.

Customers of such packages typically mount the package on an larger substrate, such as motherboard. The outer lead portions are soldered to metal traces of a mounting surface of the motherboard. The outer lead portions space the body of encapsulant
30 material (and accordingly the chip, die pad, bond wires, and inner leads) a vertical

distance above the mounting surface. Accordingly, the package has a relatively large height above the mounting surface, which is undesirable in some applications.

Lately, practitioners have attempted to make packages thinner by providing the die pad and leads at a bottom surface of the body of encapsulant material, rather than in the middle of the body of encapsulant material. Such packages enjoy a lower height than the standard leadframe packages mentioned above, since there is no encapsulant beneath the die pad and leads. Nonetheless, the height of the package above the mounting surface may still be too great for some applications, since the encapsulant must still extend over the die. Accordingly, a solution is necessary for applications where the height of the package above the mounting surface of the motherboard must be as small as possible.

SUMMARY OF THE INVENTION

A mounting for a package containing a semiconductor chip is disclosed, along with methods of making such a mounting. The mounting includes a substrate having a mounting surface with conductive traces thereon, and an aperture extending through the substrate. The package includes a base, such as a leadframe or a metallized laminate sheet, with input/output terminals for electrically connecting the package to the traces of the mounting surface. At least one chip is provided on a first side of the base of the package. The chip is electrically connected through the package (i.e., directly or indirectly) to the input/output terminals of the package. A cap, which may be a molded encapsulant material, is provided on the first side of the base over the chip. The package is mounted on the substrate so that the cap extends into the aperture of the substrate. A circumferential portion of the first side of the base outside of the cap is juxtaposed with the mounting surface so as to support the package and allow the input/output terminals of the package to be electrically connected to juxtaposed traces of the mounting surface of the substrate. Because the cap is within the aperture, a height of the package over the

mounting surface is much less than in a conventional mounting, yielding distinct advantages in applications where the height of the package over the mounting surface is critical.

Various exemplary embodiments of mountings and packages for the mountings
5 also are disclosed herein. For example, a mounting for a stack of packages is disclosed, wherein a second package is mounted on a first package that is mounted on the substrate. Alternatively, two packages may be mounted on opposite sides of the substrate, with the cap of each package in the aperture and facing the cap of the other package. In addition, embodiments for electrically connecting the package to the traces of the substrate using
10 clips on the substrate, or channels in the substrate, are disclosed. Such embodiments can allow for a snap-in, solderless electrical connection of the package to the substrate.

These and other features and aspects of the present invention will become clear upon a reading of the following detailed description of the exemplary embodiments, in conjunction with the accompanying drawings thereof.

15 BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross-sectional side view of a mounting for a package.

Fig. 2 is a cross-sectional side view of an alternative mounting for a package, wherein the mounting surface includes clips to fasten the package to the substrate.

Fig. 3 is a cross-sectional side view of a mounting for an alternative package,
20 wherein the package includes a semiconductor chip in a flip chip connection with leads of the package.

Fig. 4 is a cross-sectional side view of a mounting for an alternative package, wherein the die pad and leads of the package include a means for preventing the die pad and leads from being pulled vertically from the body of encapsulant material.

Fig. 5 is a cross-sectional side view of a mounting for an alternative package, wherein the package includes a pair of stacked, electrically interconnected chips.

Fig. 6 is a cross sectional side view of a mounting for an alternative package, wherein the package includes a central cavity for the chip and a lid over the chip.

5 Fig. 7 is a cross-sectional side view of a mounting for an alternative package, wherein the package is leadless chip carrier package.

Fig. 8 is a cross sectional side view of another alternative mounting for a package, wherein the mounting surface includes channels for insertion of the outer portion of the leads of the package therein.

10 Fig. 9 is a cross-sectional side view of another alternative mounting, wherein the mounting includes a stack of electrically interconnected packages.

Fig. 10 is a cross sectional side view of a mounting for two packages.

In the drawings, identical or similar features of the various embodiments shown therein are typically labeled with the same reference numbers.

15 DETAILED DESCRIPTION

Fig. 1 illustrates a mounting 101 in accordance with one embodiment of the present invention. Mounting 101 includes a semiconductor package 12 that is mounted on and electrically connected to an interconnective substrate 10, which may be a motherboard or some other type of electronic chassis.

20 Substrate 10 includes a core layer 14. For example, layer 14 may be a glass-fiber reinforced epoxy laminate sheet, a ceramic sheet, an insulated metal sheet, a film, or some other suitable material. Substrate 10 includes a first surface 10a and an opposite second surface 10b. A rectangular aperture 10c extends through substrate 10 between first surface 10a and second surface 10b. Conductive traces 20 (e.g., copper) are formed

on second surface 10b. (The term "conductive trace" is used broadly to include any type of conductive terminals). Traces 20 carry electrical signals to and from package 12.

Semiconductor package 12 includes a semiconductor chip 22, a metal leadframe, and a body 24 of a hardened, insulative encapsulant material. The leadframe includes a metal die pad 26 and horizontal metal leads 28. Leads 28 each include an inner lead
5 portion 30 that is within body 24, and an outer lead portion 32 that extends out of body 24 in the same horizontal plane as inner lead portion 30 and die pad 26. The leadframe may be formed of copper, copper alloy, steel, Alloy 42, or some other metal.

Chip 22 includes an active surface 22a where integrated circuit devices are
10 formed, and an opposite inactive surface 22b. Active surface 22a includes a plurality of conductive bond pads 22c along the edges of active surface 22a. Bond pads 22c may be formed along two peripheral edges or all four peripheral edges of active surface 22a. Inactive surface 22b of chip 22 may be polished to make chip 22 thinner, thereby reducing package height.

15 Body 24 has a planar first surface 24a, an opposite planar second surface 24b, and peripheral side surfaces 26c. Typically, body 24 may be formed by molding or pouring and then curing a resin material (e.g., an epoxy resin). Where body 24 is molded, as in this example, side surfaces 26c typically will be tapered to accommodate release from the mold.

20 Die pad 26 has a planar first surface 26a, an opposite second surface 26b, and peripheral side surfaces 26c. Inactive surface 22b of chip 22 is adhesively attached to first surface 26a. Second surface 26b of die pad 26 is exposed in the plane of second surface 24b of body 24. First surface 26a and side surfaces 26c of die pad 26 are covered by the encapsulant material of body 24. In an alternative embodiment, die pad 26 may be
25 set up into body 24, i.e., out of the horizontal plane of leads 28 and second surface 24b of

body 24, so that second surface 26b of die pad 26 is covered by the encapsulant material of body 24.

As mentioned, leads 28 are horizontal and include an inner lead portion 30 that is within body 24, and an outer lead portion 32 that is outside of body 24. Leads 28 have a first surface 28a, an opposite second surface 28b, and peripheral side surfaces between the first and second surfaces 28a, 28b. An inner end surface 28c of inner lead portion 30 of leads 28 faces die pad 26. The first surface 28a, peripheral side surfaces, and inner end surface 28c of inner lead portion 30 are covered with the encapsulant material of body 24. All of second surface 28b of lead 28 is exposed, including the portion of second surface 28b corresponding to inner lead portion 30. The peripheral side surfaces of inner lead portion 30 may include protruding anchor ears or the like, or an aperture may be formed vertically through inner lead portion 30, in order to prevent leads 28 from being pulled horizontally from body 24.

In a typical process for making package 12, a metal strip including an array of identical leadframes is processed in parallel. After each chip 22 is mounted on the die pad 26 of one of the leadframes and is electrically connected to the leads 28 of the respective leadframe, a body 24 is individually formed (e.g., molded) over each chip 22 and leadframe of the array. After the encapsulant material is cured, individual packages 12 are singulated from the metal strip by punching or sawing through the outer lead portion 30 of the leads 28 at a selected distance (e.g., 0.1 to 0.2 mm) from side surface 24c of body 24.

Practitioners will appreciate that package 12 has a reduced height, compared to the first conventional package mentioned above, because die pad 26 and leads 28 are provided at second surface 24b of package body 24.

Package 12 is electrically connected to traces 20 of second surface 10b of substrate 10 so that electrical signals may be passed between substrate 10 and chip 22 of package 12. In particular, each bond pad 22c of chip 22 is electrically connected by a conductor, e.g., a metal wire 34 made of gold or aluminum, to a first surface 28a of an inner lead portion 30 of a lead 28. Low loop bond wires or TAB bonds may be used to help reduce package height. In addition, the first surface 28a of each outer lead portion 30 is electrically connected by a conductor, such as metal solder 36, to metal traces 20 of substrate 10. Of course, these electrical connections may vary. For example, a conductive adhesive material, such as a metal-filled epoxy, may be used instead of solder 36 to electrically connect outer leads 32 to metal traces 20.

Package 12 is mounted on substrate 10 in a manner that significantly lessens a height of package 12 above second surface 10b of substrate 10, on which package 10 is mounted. In particular, package 12 is mounted so that most of body 24 of package 12 is within aperture 10c of substrate 10. First surface 24a of body 24 and a majority portion of side surfaces 24c of body 24 are within aperture 10c. Only die pad 26, leads 28, and second surface 24b of body 24 are above second surface 10b of substrate 10, thereby accomplishing a very low mounting height.

The height of package 10 of mounting 101 above second surface 10b of substrate 10 is about equal to the height (i.e., thickness) of die pad 26 and leads 28. In comparison to conventional mountings, height savings are realized by providing body 24 of package 10 within aperture 10c, providing die pad 26 and leads 28 at second surface 24b of body 24 rather than in the middle of body 24, and, if desired, by thinning chip 22 and by using low-loop height bond wires 34.

If desired, an additional electronic device (e.g., a package containing a chip, or a passive device such as a capacitor, resistor, or inductor) may be placed on package 12 and

electrically connected thereto so that there is an electrical connection between the electronic device and second surface 28b of some or all of the leads 28, thereby electrically connecting package 12 to the additional electronic device.

Fig. 2 depicts a mounting 102 in accordance with another embodiment of the present invention. Mounting 102 is nearly the same as mounting 101 of Fig. 1, and thus does not need to be discussed in redundant detail. In mounting 102 of Fig. 2, clips 11 are provided on second surface 10b of substrate 10 adjacent to aperture 10c. Clips 11 each include an electrically conductive portion that is electrically connected to one of the traces 20 of second surface 10b. For example, each clip 11 may be metal, and may be soldered to one of the traces 20. Outer leads 32 of package 12 each snap into a respective one of the clips 11, thereby electrically connecting package 12 to substrate 10 without a soldered or otherwise adhesive connection.

Fig. 3 depicts a mounting 103 in accordance with another embodiment of the present invention. The difference between mounting 103 of Fig. 3 and mounting 101 of Fig. 1 is in the configuration of package 12. In contrast to Fig. 1, inner lead portion 30 of each lead 28 of package 12 of Fig. 3 is made longer, and the area of die pad 26 is reduced so as to fit within a boundary defined by bond pads 22c. Moreover, chip 22 is mounted in a flip chip style on first surface 26a of die pad 26 and first surface 28a of the inner lead portions 30. An insulative adhesive is used to attach first surface 22a of chip 22 to first surface 26a of die pad 26. Bond pads 22c of chip 22 face first surface 28a of the inner lead portions 30 and are electrically connected thereto with a conductive metal solder (e.g., a gold solder) or a conductive adhesive. In an alternative embodiment, die pad 26 may be omitted, such that chip 22 is supported in a flip chip style solely on first surface 28a of leads 28. In such an embodiment, encapsulant material of body 24 would fill in under active surface 22a of chip 22.

Fig. 4 depicts a mounting 104 in accordance with another embodiment of the present invention. Again, the difference between mounting 104 of Fig. 4 and mounting 101 of Fig. 1 is in the configuration of package 12. Die pad 26 and leads 28 of package 12 of Fig. 4 include a means for preventing die pad 26 and leads 28 from being pulled
5 vertically from body 24. On die pad 26, this vertical locking feature includes an undercut region 26d at the periphery of die pad 26 that extends fully around, or extends at least along two opposing edges of, die pad 26. On leads 28, this vertical locking feature includes an undercut region 28d in second surface 28b of inner lead portion 30. Encapsulant material of body 24 fills in under undercut region 26d of die pad 26 and
10 undercut region 28d of inner lead portion 30. The underfilled encapsulant material supports die pad 26 and leads 28 in body 24. Undercut regions 26d and 28d may be formed by masking and then etching about half way through the thickness of die pad 26 and leads 28 in the regions shown. In this regard, the reader is referred to U.S. Patent Application 09/176,614 , which is incorporated herein by reference in its entirety.

15 Alternatively, instead of having half-etched regions, die pad 26 and leads 28 may have a stamped or coined circumferential lip at first surface 26a of die pad 26 and first surface 28a of lead 28. The lip circumscribes die pad 26, and extends along the side surfaces and inner end surface 28c of each lead 28. The lip ultimately is underfilled by encapsulant material of body 24, thereby vertically locking die pad 26 and leads 28 to
20 body 24. Alternatively, side surfaces 26c of die pad 26 and the side surfaces and inner end surface 28c of leads 28 may include a central peak that extends into the encapsulant material or a central depression that is filled by the encapsulant material. In this regard, the reader is directed to U.S. Patent No. 6,143,981, which is incorporated herein by reference in its entirety.

Fig. 5 depicts a mounting 105 in accordance with another embodiment of the present invention. Again, the difference between mounting 105 of Fig. 5 and mounting 101 of Fig. 1 is in the configuration of package 12. In particular, package 12 of Fig. 5 includes two chips 22 (e.g., two semiconductor memory chips) stacked one on top of the other. A spacer 40 is attached between the active surface 22a of a first chip 22 and the inactive surface 22b of a second chip 22 stacked on the first chip 22. Spacer 40 is fully within a perimeter defined by the bond pads 22c of the first chip 22, and spaces the second chip 22 above the bond wires 34 that are bonded to the bond pads 22c of the first chip 22. Spacer 40 may be formed of silicon with an insulative adhesive material coated on its opposing major surfaces, among other possibilities. The first and second chips 22 are electrically connected with each other through pairs of bond wires 34 that are connected to the same leads 28 of package 12. Alternatively, an adhesive film or a thick glob of an adhesive material may be between the chips so as to space them apart and attach them together.

Fig. 6 depicts a mounting 106 in accordance with another embodiment of the present invention. Again, the difference between mounting 106 of Fig. 6 and mounting 101 of Fig. 1 is in the configuration of package 12. In particular, package 12 of Fig. 5 provides a cavity 24d in body 24. First surface 26a of die pad 26 and first surface 28a of inner lead portion 30 of the leads 28 are exposed in cavity 24d. After forming body 24, a chip 22 is placed on first surface 26a of die pad 26 in cavity 24d, and is wire bonded to the exposed surface 28a of leads 28. A lid 42 is attached to the rim of cavity 24, thereby closing cavity 24d. Such a package may be appropriate where chip 22 is an optical device, in which case lid 42 is optically clear so as to transmit light to an optical cell on active surface 22a of chip 22. Alternatively, an optically clear encapsulant can be provided in cavity 24d in place of having a lid 42. Having a cavity 24d in body 24 also is

appropriate where chip 22 is a micromachine or some other chip that cannot covered by an encapsulant material.

Fig. 7 depicts a mounting 107 in accordance with another embodiment of the present invention. Again, the difference between mounting 107 of Fig. 7 and mounting 5 101 of Fig. 1 is in the configuration of the package. In mounting 107 of Fig. 7, package 50 includes a substrate 52 that includes a layer of insulative material 54 (e.g., a polyimide film, a glass-fiber reinforced laminate sheet, or ceramic) upon which metal circuit patterns 56 are formed. A body 24 of an insulative encapsulant material is provided over a central region of a first surface 52a of substrate 52. A peripheral region of first surface 10 52a around body 24 is free of the encapsulant material. Chip 22 is attached to a metal die pad 55 on first surface 52a and is electrically connected to an encapsulated inner end 56a of the circuit patterns 56. An outer end 56b of each circuit pattern 56 is exposed at the periphery of first surface 52a outside of body 24. The outer end 56b of each circuit pattern 56 of package substrate 52 serves as an input/output terminal of package 50.

15 Body 24 of package 50 is positioned in aperture 10c of mounting substrate 10, just as in Fig. 1. The peripheral region of first surface 52a of substrate 52 is supported on first surface 10a of substrate 10 around aperture 10c. Outer end 56b of each of the circuit patterns 56 is connected by solder 36 or the like to one of the traces 20 on first surface 10a of substrate 10, thereby forming an electrical connection between package 50 and 20 substrate 10. Accordingly, package 50 of mounting 107 has a very low height above second surface 10b of substrate 10. The height of package 50 of mounting 107 is approximately equal to the thickness of substrate 52 of package 50, since body 54 is in aperture 10c.

If desired, package 50 may include further metal input/output terminals 58 on 25 second surface 52b of substrate 50. Input/output terminals 58 are electrically connected

by vias 60 through substrate 50 to circuit patterns 56 on first surface 52a. Accordingly, another package could be stacked on second surface 52b if desired, and electrically connected to package 50 (and hence to substrate 10) through terminals 58.

In an alternative embodiment, package 50 may include a rectangular central
5 aperture through substrate 52 within which chip 22 is located. In such a package, chip 22 would be supported and connected to substrate 52 by the encapsulant material of body 24. Such a package enjoys a very thin profile because chip 22 is in an aperture of substrate 52.

Fig. 8 depicts a mounting 108 in accordance with another embodiment of the
10 present invention. The difference between mounting 108 of Fig. 8 and mounting 101 of Fig. 1 is in the connection of package 12 to substrate 10. In particular, substrate 10 of Fig. 8 includes a plurality of metal-lined channels 10d in second surface 10b around aperture 10c. The metal lining of each channel 10d is electrically connected to a trace 20 of first surface 10a. Channels 10d are formed so that outer leads 32 of package 10 can be
15 fitted or snapped therein, thereby forming a solderless electrical connection between package 12 and substrate 10. Depending on the tightness of the fit, solder may be applied over leads 32 to make a more secure electrical connection to the metal lining of the respective channels 10d. Accordingly, with body 24 in aperture 10c and each outer lead 32 in a channel 10d, second surface 24b of body 24 of package 10 may be flush with or
20 nearly flush with second surface 10b of substrate 10, depending on the depth of the channels 10b.

Fig. 9 depicts a mounting 109 in accordance with another embodiment of the present invention. In mounting 109, a second package 12 is stacked on the package 12 of Fig. 1 that is mounted on substrate 10. In particular, second surface 24b of body 24 of the
25 upper package 12 is juxtaposed with and supported on the second surface 24 of body 24

of the lower package 12. Moreover, the exposed second surface 28b of each lead 28 of the upper package 12 is juxtaposed with and electrically connected by solder 36 or the like to the exposed second surface 28b of one of the leads 28 of the lower package 12, thereby electrically connecting the stacked packages 12. With the body 24 of the lower package 12 in aperture 10c of substrate 10, the height of the stack of packages 12 above mounting surface 10b of substrate 10 is less than the sum of the heights of the two packages 12 unstacked. Further reductions in height may be obtained, for example, by using channels 10d in substrate 10, as shown in Fig. 8. Mounting 109 may be made by mounting a first package 12 on substrate 10, as in Fig. 1, and then mounting a second package 12 on the first package 12. Alternatively, the two packages 12 can be electrically connected in a stack prior to electrically connecting the stack to substrate 10. In one application, the two packages may include identical memory chips, with one package arranged to be the mirror image of the other so that the chips therein may be electrically connected in parallel.

15 Fig. 10 depicts a mounting 110 in accordance with another embodiment of the present invention. Mounting 110 is the same as mounting 101 of Fig. 1, except that two packages 12 are independently mounted on opposing sides of substrate 10. In particular, a first package 12 is mounted on the surface 10b of substrate 10, as in Fig. 1, and a second package 12 is mounted on first surface 10a of substrate 10. The body 24 of each package 12 is in aperture 10c, such that their respective first surfaces 24a are juxtaposed. Substrate 10 must be sufficiently thick in this embodiment that each package will fit within aperture 10c. If desired, the two packages 10 may be electrically interconnected by providing metal vias through substrate 10 between the respective metal traces 20 of first surface 10a and second surface 10b. With both packages 12 in aperture 10c, a low

combined height above mounting surfaces 10a, 10b is achieved while doubling the mounting density.

Practitioners will appreciate that the embodiments described herein are exemplary only, and not limiting. The present invention includes all that fits within the literal and
5 equitable bounds of the claims.